

Fig. 1

0002227-1-5434250

FIG. 2

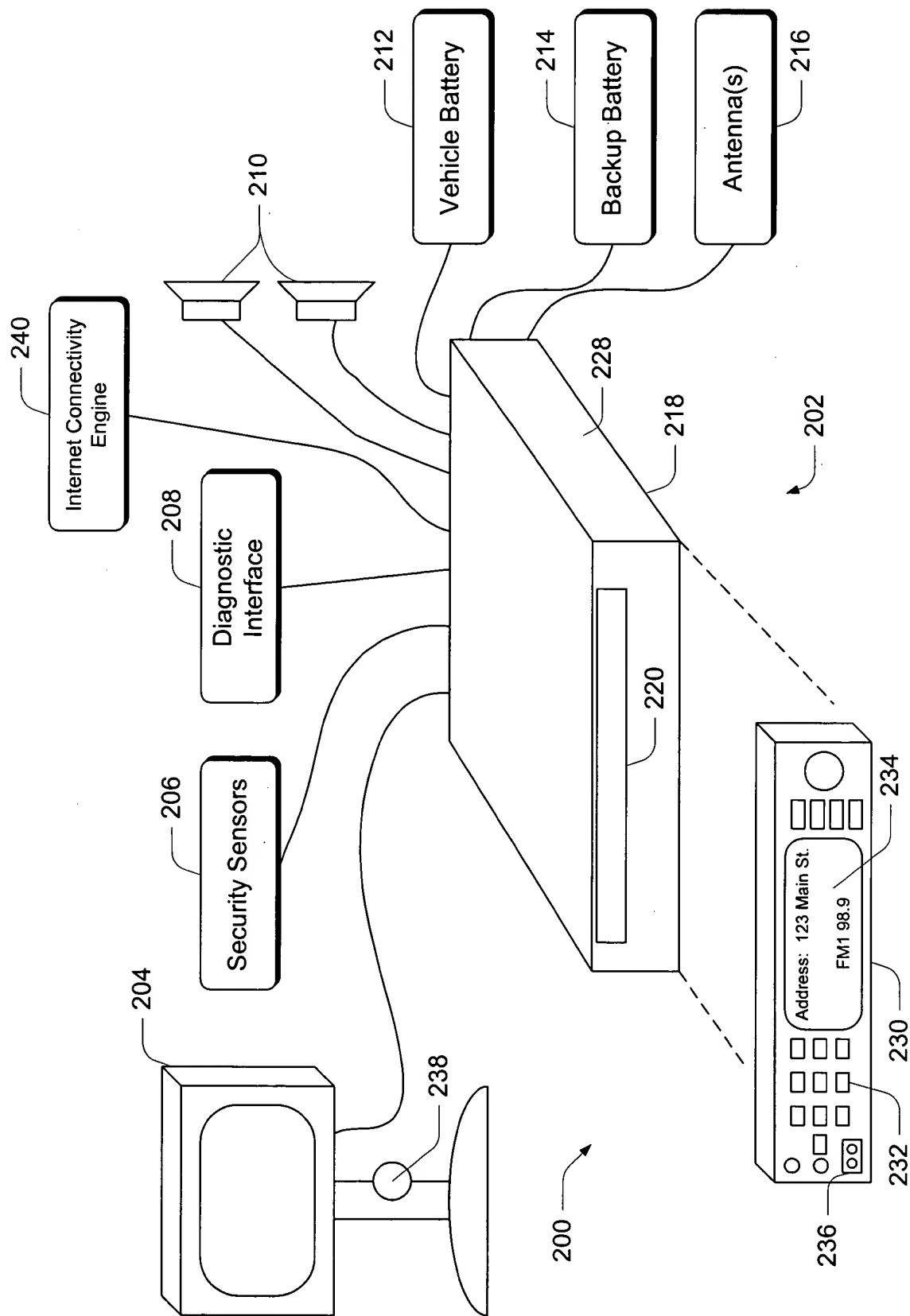


Fig. 2

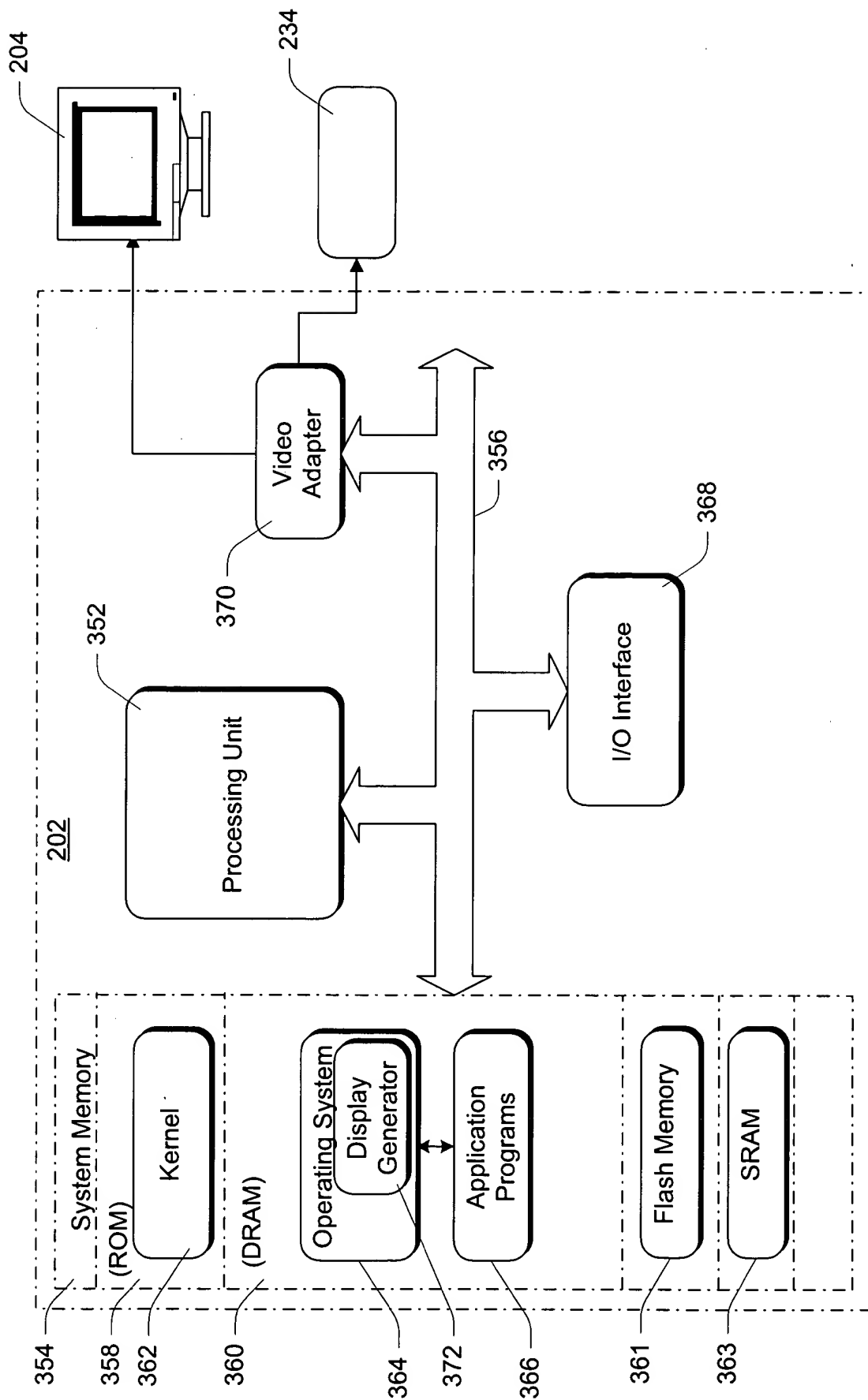
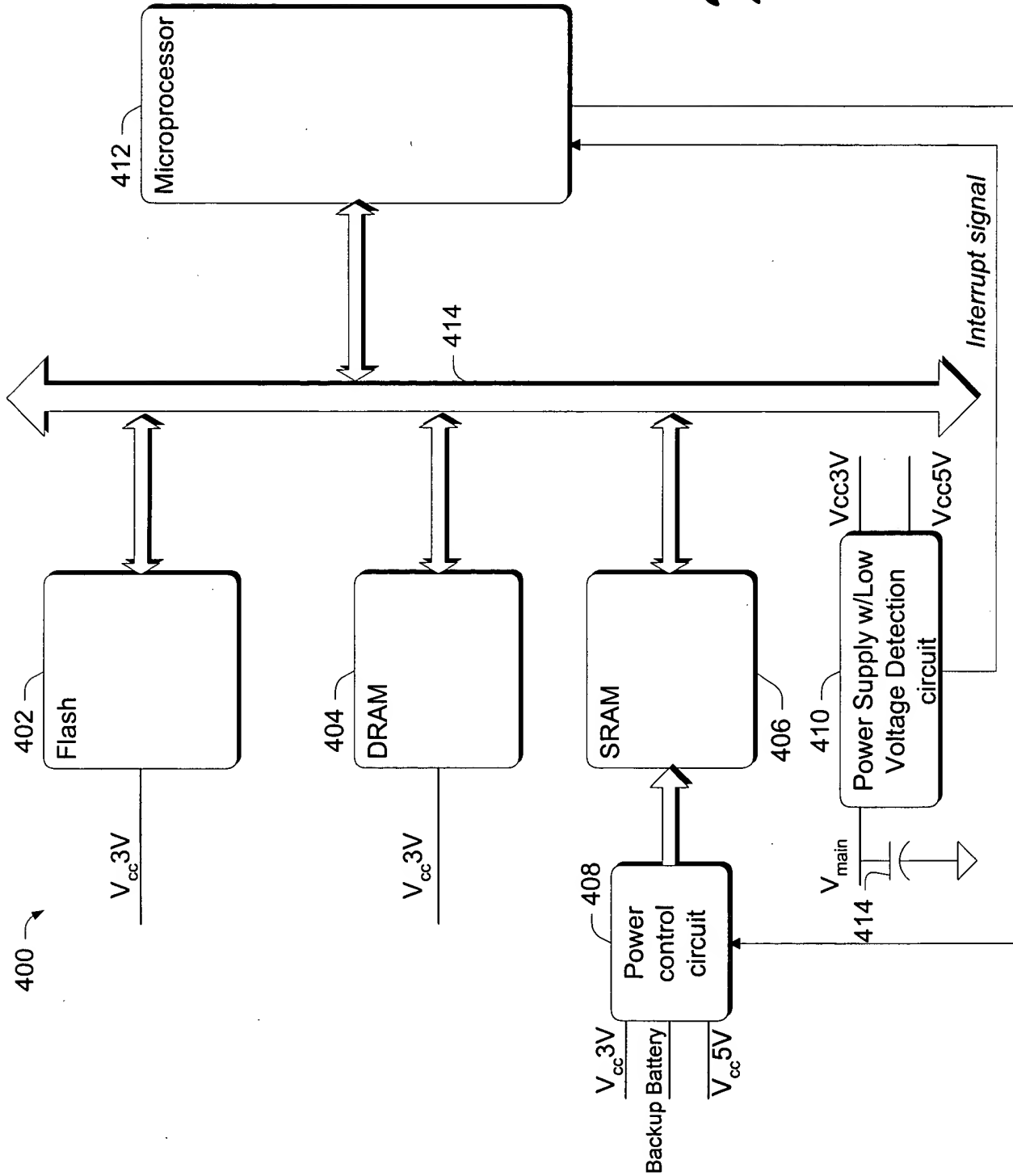


Fig. 3

Fig. 4



0000227" 43434260

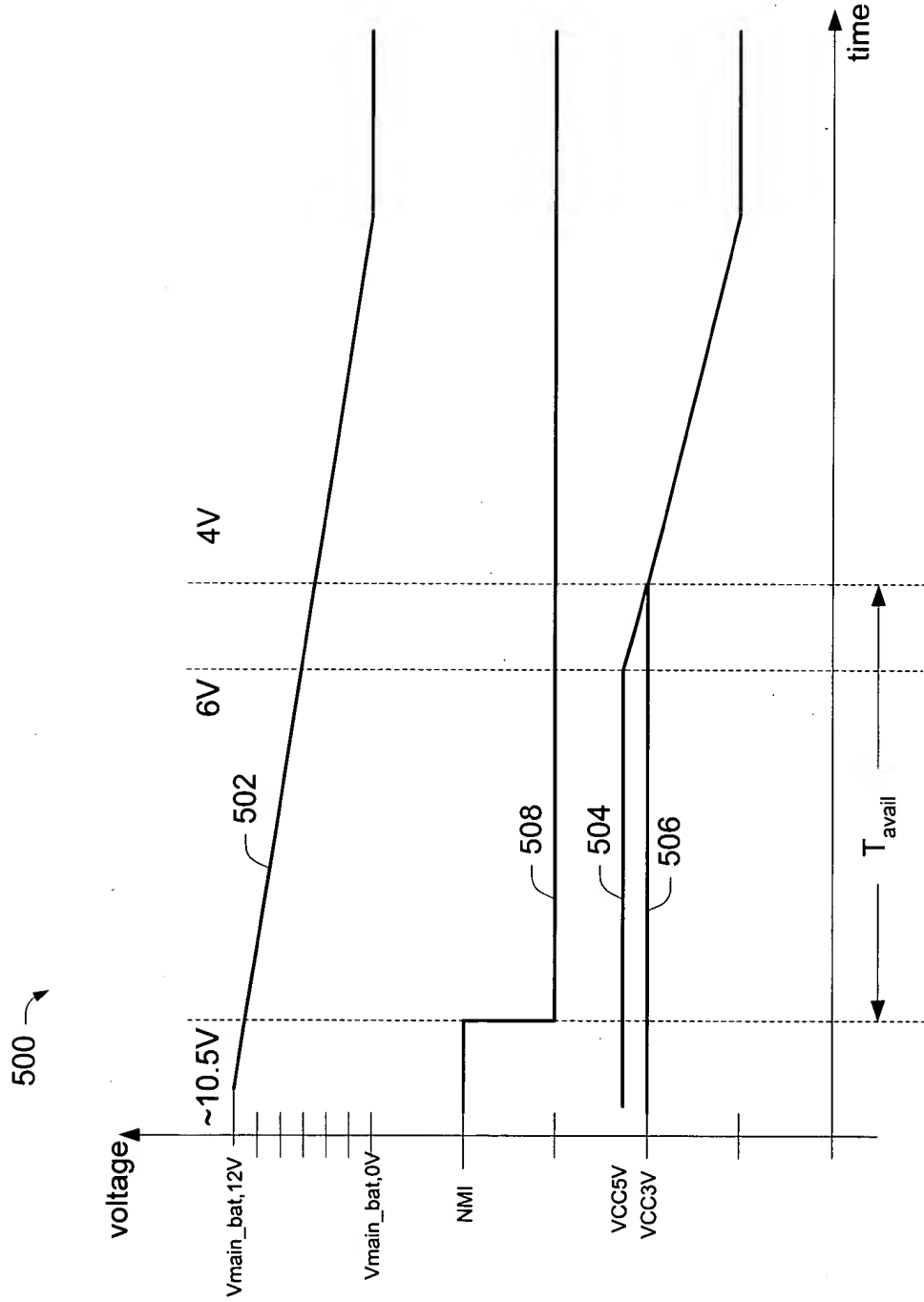


Fig. 5

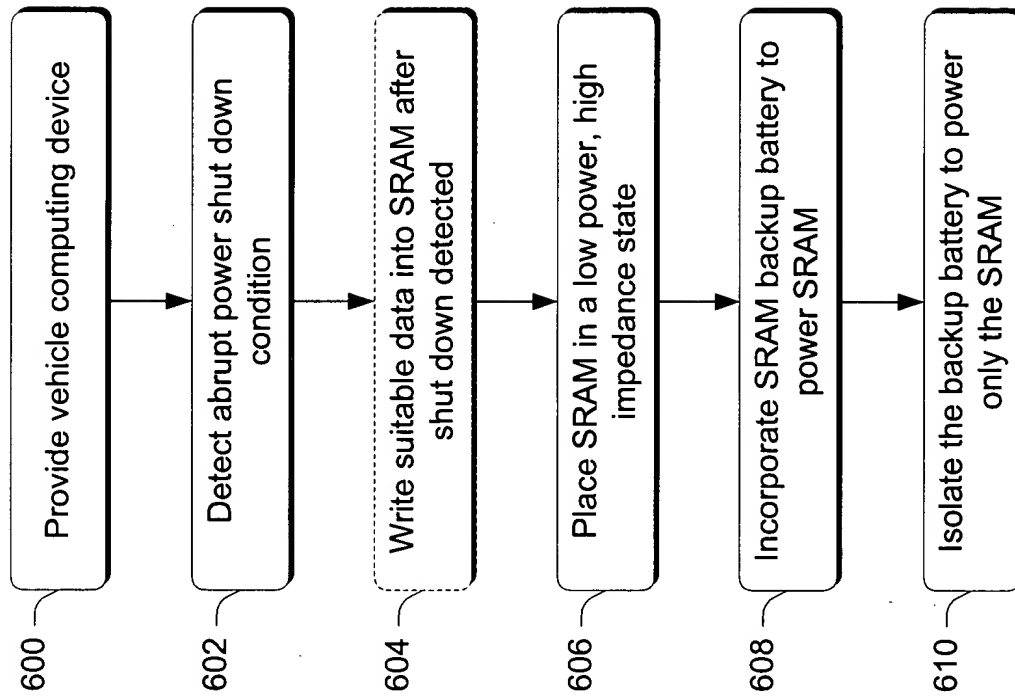


Fig. 6

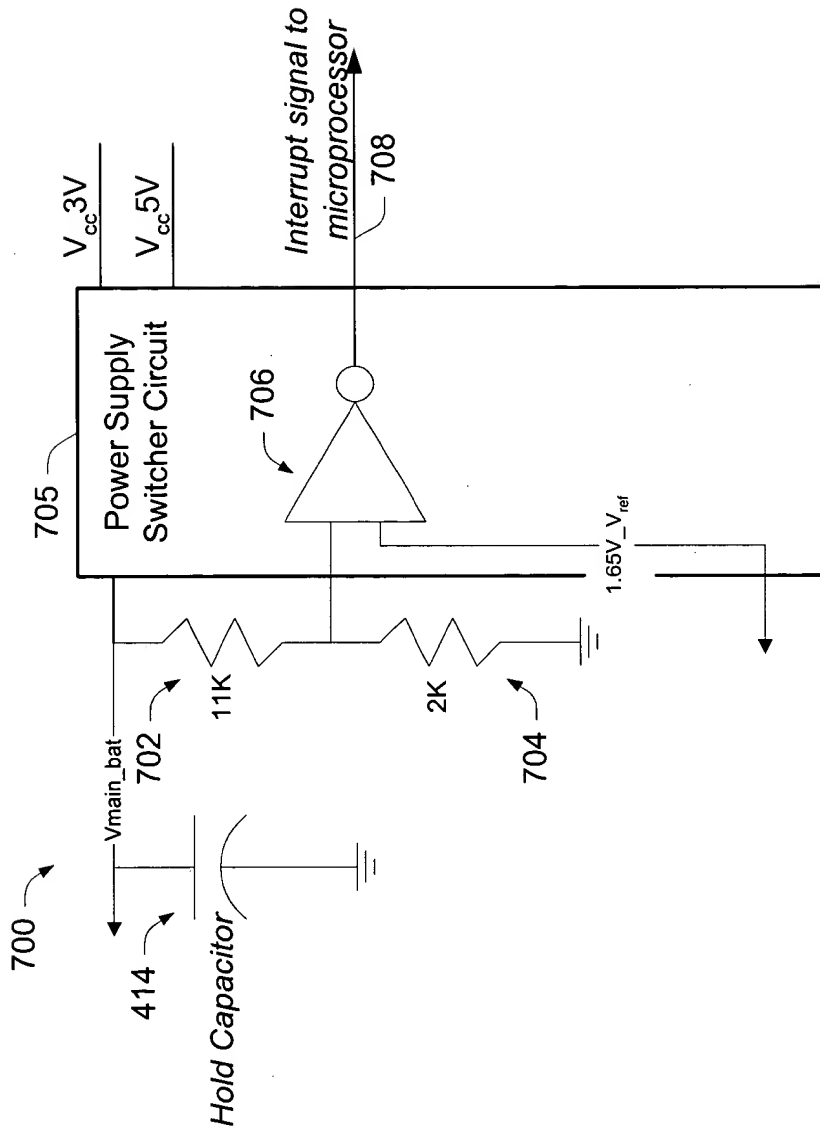


Fig. 7



Fig. 8

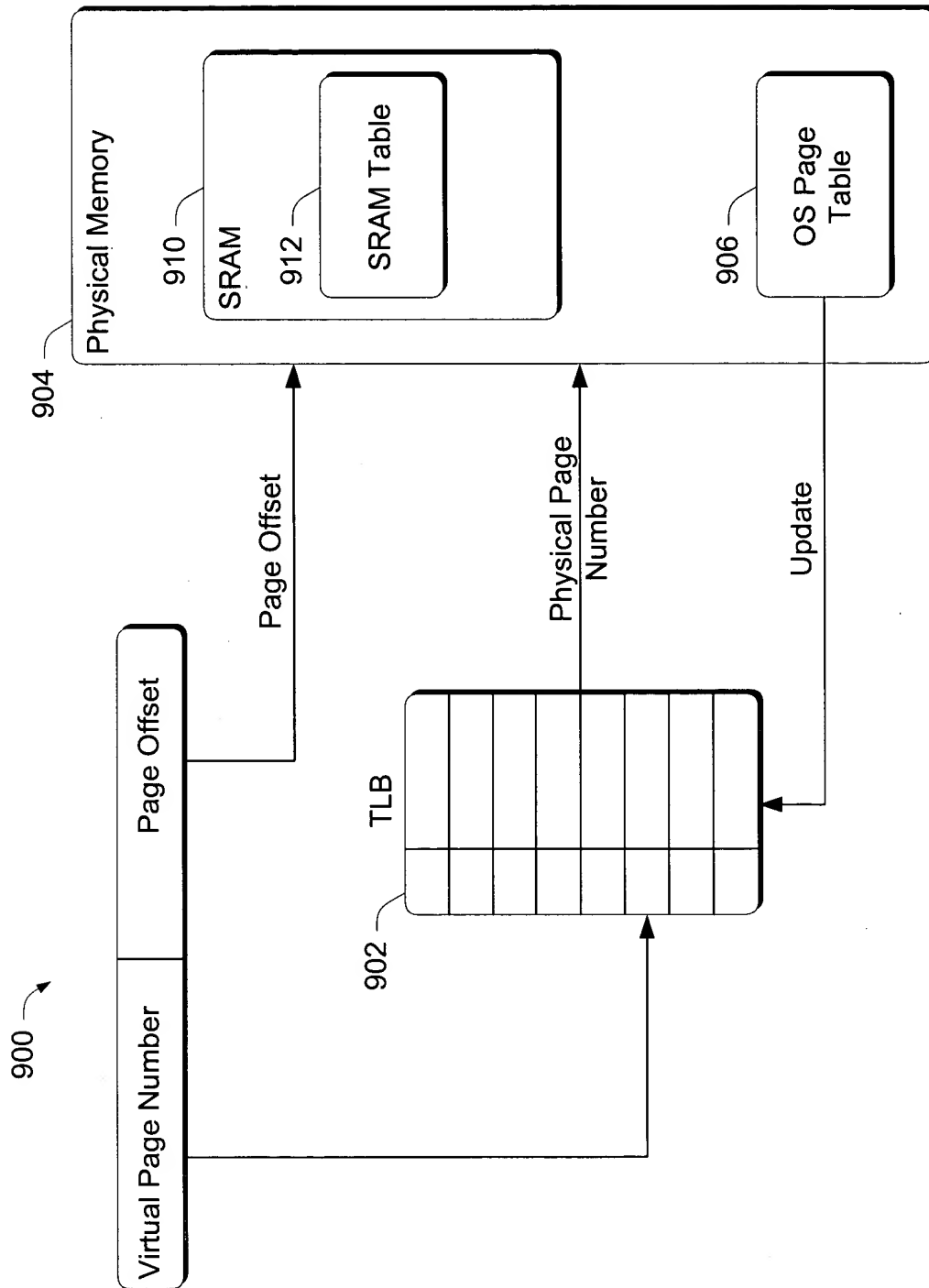


Fig. 9

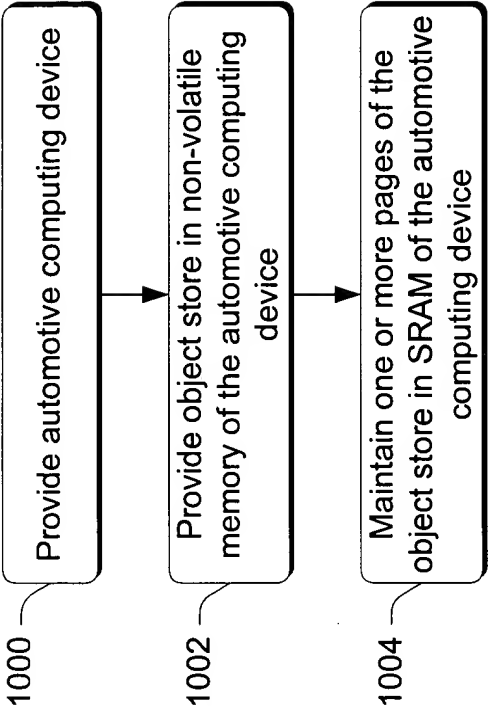


Fig. 10

1100

L = Location (SRAM, DRAM, or Flash) bits (2 bits)

P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	M	M	M	M	M	M	M	M	M	M	L	L	D
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

P = DRAM Address bits (14 bits)

M = Address bits tracking page's current location (14 bits)

D = Page Dirty bit (1 bit)

F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	N	N	N	N	N	N	N
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

F = Flash Address bits (14 bits)

N = Number of Times Page Has Been Written to Flash (8 bits)

Fig. 11

Handling Object Store Page Exception

Exception Type	Current Access for OS page	Current Location of OS page	Action	Additional Notes
Write	Write	SRAM	No special action is required. This is a normal TLB miss. OS page table information must be fetched and stored inside the TLB. No interaction with the SRAM object store page table is required	Since the TLB has a limited number of entries, repeated page table misses can happen often
Read	Read	DRAM or SRAM	No special action is required. This is a normal TLB miss. OS page table information must be fetched and stored inside the TLB. No interaction with the SRAM object store page table is required	Since the TLB has a limited number of entries, repeated page table misses can happen often
Read	Read	Flash	<p>(1) Copy the page into DRAM at physical address specified in the OS page table. (The faulting virtual address is used as a key into the OS page table in which the corresponding physical address is stored).</p> <p>(2) Modify the OS page table and TLB permissions for read-only accesses.</p> <p>(3) Copy the M bits to the F bits in order to specify where the page is located in flash in case of power loss. Modify the L bits to indicate that the page is now in DRAM.</p> <p>(4) Modify the SRAM object store page table M bits to specify the physical address in DRAM.</p>	<p>The access bits are changed to read only so that an attempt to write to the page will cause a write exception. In this exception handler, the page can be copied to SRAM before writing to it (thus making it dirty).</p>

Fig. 12

Fig. 12 (cont.)

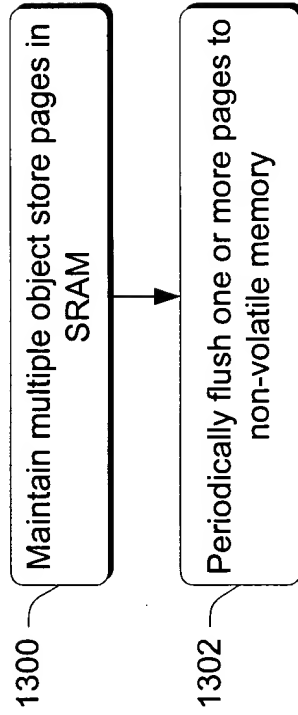


Fig. 13

1400 ↗

Before Compaction

Block 0 used page A
Block 0 unused page
Block 0 unused page
Block 0 unused page
Block 1 used page B
Block 1 unused page
Block 1 unused page
Block 1 unused page

After Compaction (with a free block added)

Block 0 unused page
Block 0 unused page
Block 0 unused page
Block 0 unused page
Block 1 unused page
Block 1 unused page
Block 1 unused page
Block 1 unused page
Block 2 used page A
Block 2 used page B
Block 2 new page
Block 2 unused page

1402

Fig. 14



Fig. 15

1600 →

After Compaction

Block 0 page A
Block 0 page C
Block 0 page D
Block 0 new page
Block 1 free block
Block 1 free block
Block 1 free block
Block 1 free block
Block 2 page E
Block 2 unused but not erased
Block 2 page G
Block 2 page H

Before Compaction

Block 0 <free block page>
Block 0 <free block page>
Block 0 <free block page>
Block 0 <free block page>
Block 1 page A
Block 1 unused but not erased
Block 1 page C
Block 1 page D
Block 2 page E
Block 2 unused but not erased
Block 2 page G
Block 2 page H

Fig. 16

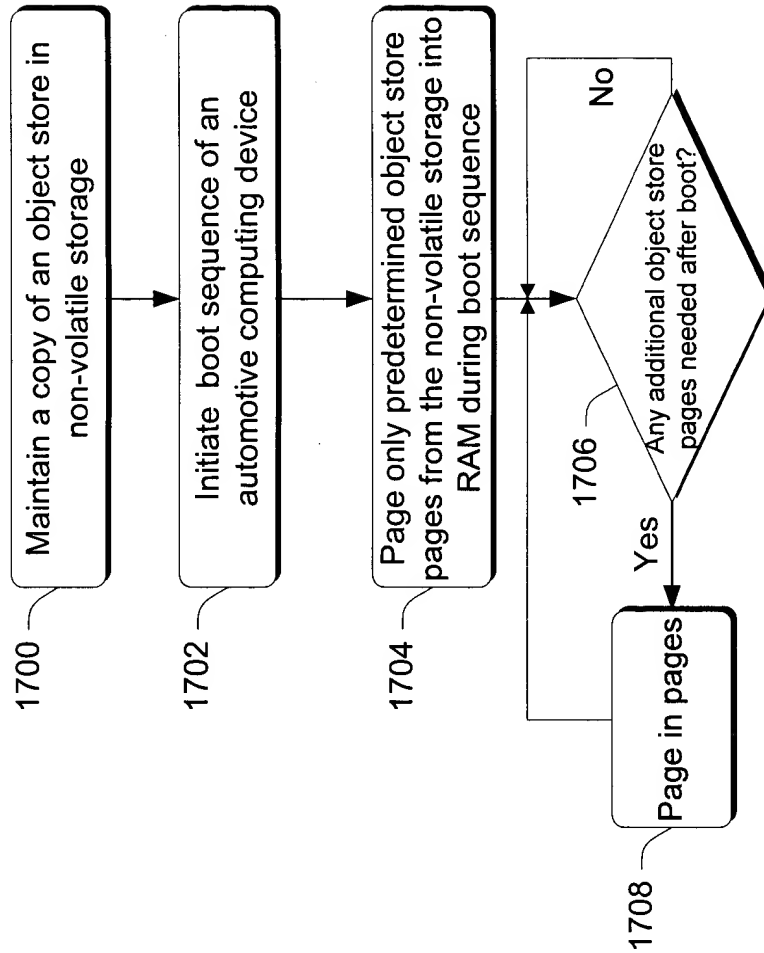


Fig. 17